MULTIMEDIA UNIVERSITY ™

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2017/2018

EEE1036 – DIGITAL LOGIC DESIGN

(All sections / Groups)

04 JUNE 2018
9.00 a.m - 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 6 pages with 4 questions only.
2. Answer all **FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1 (25 marks)

(a) Name the conversion process used to convert an analog signal to the corresponding digital signal. Describe how this process is used to convert the following analog voltage signal in **Figure 1(a)** to its corresponding 4-bit digital signal representation. Assume the analog voltage ranges between +8V to -8V. [5 marks]

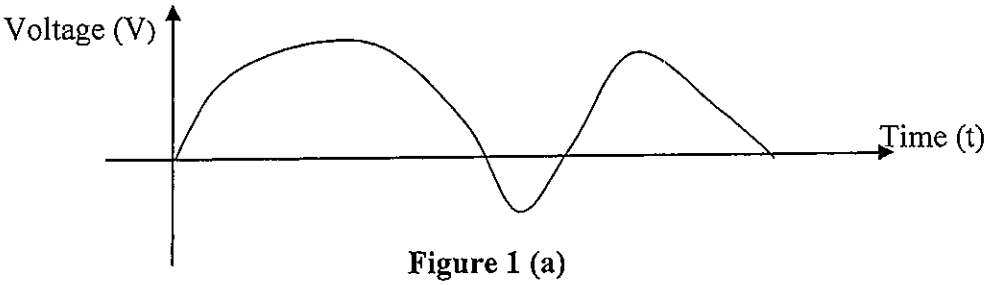

Figure 1 (a)

(b) Convert and complete the given numbers in **Table Q1** to other specific bases listed. Reproduce this table in your answer sheet and show **COMPLETE** working steps for each conversion.
[Remarks: Do not carry out any truncation of digits during the conversions.]

Table Q1

	Base-2	**Base-4**	**Base-8**	**Base-10**	**Base-16**
Integer		123			
Fractional					0.AE

[12 marks]

(c) Perform the following operations in 8-bit two's complement notation for both the operands and result. Justify for any discrepancy.

(i) Subtract 45_{10} from -75_{10} [2 marks]

(ii) Add 86_{10} to 71_{10} [2 marks]

(d) Perform the following operations:

(i) BCD addition for 87_{10} and 35_{10}. [2 marks]

(ii) Convert binary number 11010010101_2 to Gray code. [2 marks]

Continued...

Question 2 (25 marks)

(a) Simplify the following Boolean expression below:

$$\left[W\overline{X}(Y+XZ)+\overline{W}\,\overline{X}\right]Y$$

[4 marks]

(b) Given the logic circuit as shown in **Figure 2(b)**:

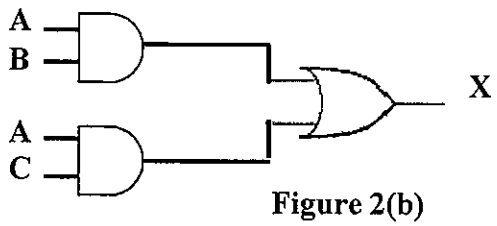

Figure 2(b)

(i) Write the logic expression for logic circuit in **Figure 2(b)**. [2 marks]

(ii) Express logic expression in part (i) in canonical Sum of Products (SOP) form. [2 marks]

(iii) Draw the truth table for **Figure 2(b)** using the results obtained from Question 2(b) (ii). [2 marks]

(c) Find the minimum Sum of Products (SOP) logic expression of output Y using Karnaugh map for the truth table in **Table Q2.** [6 marks]

Table Q2

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

(d) Determine the minimum Sum-of-Products (SOP) form with 'don't care' conditions using the Quine-McCluskey method for the following functions. List all possible minimized solutions.

$$f(A,B,C,D) = \Sigma m\,(1,6,7,9,12) + d(8,11,15)$$

[9 marks]

Continued...

Question 3 (25 marks)

(a) Redraw the given clock with edge triggered of SR input in **Figure 3(a)** and sketch the *Q* output waveform response for each edge-triggered of these flip-flops. Assume the initial condition for all Q is low.

(i) positive-edge-triggered S-R [3 marks]

(ii) negative-edge-triggered S-R [3 marks]

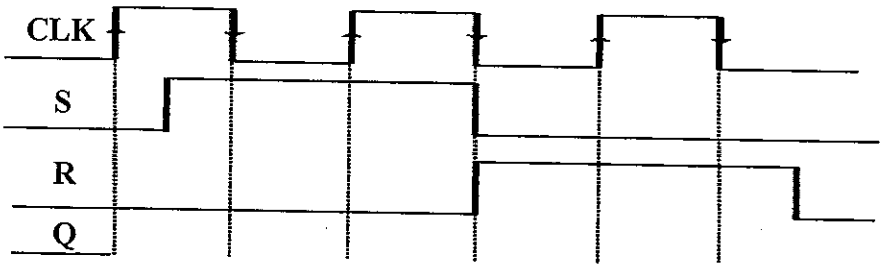

Figure 3 (a)

(b) The ripple counter using JK flip flops are shown in **Figure 3 (b)**. Redraw the complete timing diagram for eight clock pulse and show the Q_0 and Q_1 waveform. [4 marks]

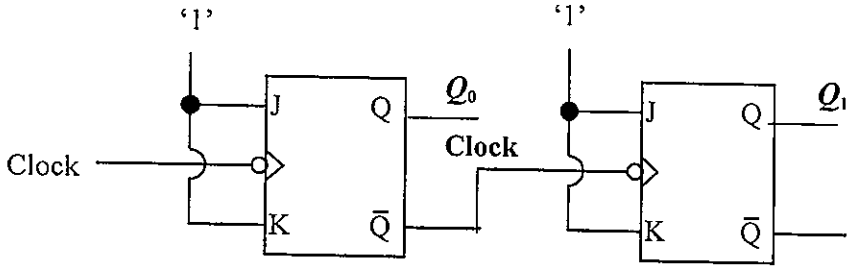

Figure 3 (b)

Q_0

Q_1

Continued...

(c) A synchronous counter using D flip flops have the following sequence: 000, 010, 101, 110, and repeat as shown in **Figure 3(c)**. The undesired (unused) states 001, 011, 100 and 111 must always go to RESET states in their NEXT states. In order to complete the design, answer the following:

(i) Draw the D flip flop truth table. [2 marks]

(ii) Produce a transition state table using the D flip flop truth table. [4 marks]

(iii) Produce Karnaugh maps and logic expressions for flip flop inputs from the transition state table. [6 marks]

(iv) Design and sketch the counter using negative-edge triggered D flip-flop. [3 marks]

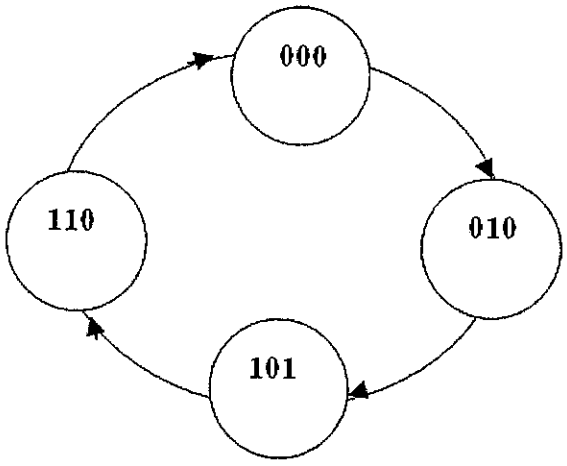

Figure 3(c)

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Question 4 (25 marks)

(a) Draw the **truth table** of 1-bit full adder. [3 marks]

(b) Extend a 3-bit full adder, by adding external logic gates, to handle addition and subtraction of two's complement numbers. Draw the schematic diagram. [3 marks]

(c) With the aid of a schematic diagram (please draw), **propose a way** to connect 6 sensors with binary output to one input port, such that the sensors' state can be read via the input port. Use arrows to show the directions of signal flow. [5 marks]

(d) With the aid of a schematic diagram (please draw), **propose a way** to connect three 4 kbytes (12-bit address) memory modules to a 15-bit address bus, such that they collectively provide 3×4 kbytes of memory space. [5 marks]

(e) **Implement** switching function $f(x,y,z)=\sum m(0,1,3,4,6,7)$ using each of the following:

(i) 3-to-8 decoder with active high outputs (draw the schematic diagram)

(ii) 4-to-1 multiplexer (draw the truth table and schematic diagram)

Let x be the most significant bit and z be the least significant bit. [9 marks]

End of Paper